REMARKS/ARGUMENTS

Claims 16-36 are pending, and are unamended.

This Office Action was issued pursuant to the remand of the application by the Board of Patent Appeals and Interferences to the Examiner to allow for the clarification of the file record by the Examiner with respect to the rejections previously advanced and for the Examiner to reconsider the claimed subject matter in light of the Board's comments. More specifically, for any rejections that may be maintained upon reconsideration by the Examiner in light of the remand, a full explanation by the Examiner as to how that prior art is being applied in any such rejections on a claim by claim basis and with full consideration of all limitations of each claim should be furnished by the Examiner.

In rejecting the claims, the Examiner relies on Onuki et al. for allegedly disclosing maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al., however, specifically discloses terminating the sputtering power during application of the bias voltage.

The Examiner points to Fig. 1(a) in Onuki et al. for the disclosure of maintaining the application of the sputtering power while biasing the plasma toward the substrate. In the Advisory Action dated January 5, 2001, the Examiner asserts: "It has been well demonstrated that Onuki et al teach the method limitations of claim 16 with reference to Fig. 1a,b. Fig. 1a,b teach both zero and non-zero bias voltages repeated between 1 and 18 cycles providing multiple layers (Section 2.1)."

Fig. 1b clearly shows **no** overlap between the bias voltage and the sputtering power. Fig. 1a merely shows a conventional DC sputtering with 4kW sputtering power and zero bias voltage, and conventional DC bias sputtering with 4kW sputtering power and –200V bias voltage. Nothing in Onuki et al., however, teaches or suggests combining or alternating the conventional DC sputtering and DC bias sputtering. As to the 18 cycles mentioned in the

Examiner's statement, Onuki et al. actually states: "In the case of one-step switching bias sputtering, a cycle consisted of 5 s d.c. and 5 s d.c. bias sputtering. A cycle was repeated 18 times for the formation of 0.5 μm thick Al-0.5wt.%Cu-1wt.%Si films." This relates to the one-step switching bias sputtering shown in Fig. 1b in which there is **no** overlap between the sputtering power and the bias voltage. It has nothing to do with the conventional DC sputtering and conventional DC bias sputtering shown in Fig. 1a. Clearly, the Examiner has misconstrued Onuki et al.

Claim 16

Claim 16 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onuki et al. To sustain a Section 102(b) rejection, the Examiner must establish that the reference discloses every element of the claim. In this case, Onuki et al. does not disclose or suggest every element of claim 16.

Onuki et al. discloses a switching bias sputtering process whereby d.c. sputtering and d.c. bias sputtering are operated alternately (page 182, right column, lines 9-11). As illustrated in Figs. 1 and 2, the switching bias sputtering process involves alternating step pulses of sputtering power and bias voltage. The step pulses of sputtering power and bias voltage alternate, and do not overlap in time. The use of the switching bias sputtering method is intended to enhance the step coverage and quality of Al films (page 182, right column, lines 12-13).

As discussed above, Onuki et al. does not disclose or suggest maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage.

The Examiner misconstrues Onuki et al., including the teachings of Fig. 1a,b, to arrive at the erroneous conclusion that Onuki et al. anticipates claim 16. Claim 16 recites depositing a first layer by sputtering without biasing the plasma and then depositing a second

layer over the first layer by sputtering and biasing the plasma. Onuki et al. clearly does not teach depositing the two different layers. Nor does Onuki et al. recognize that the first layer formed without biasing the plasma is a reduced stress layer for reducing the stress of films deposited on the substrate (Page 4, lines 1-3 and Abstract). Therefore, claim 16 is novel and patentable over Onuki et al.

Claims 17, 18, 25-28, and 32-34

Claims 17, 18, and 25-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al. Claim 30 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al.

The Examiner recognizes that Ye et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

The remaining references do not cure the defects of Ye et al. and Onuki et al. The Examiner cites Boys et al. merely for allegedly disclosing a programmable memory controller for controlling a plasma deposition system. Ramarotafika et al. describes the influence of d.c. substrate bias on the resistivity, composition, crystallite size, and microstrain of WTi and WTi-N films. None of them teach or suggest depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. The references are directed to very different processes for forming different films to achieve different purposes. For example, Onuki et al. is

directed to forming sputtered Al and Al alloy films using switching bias sputtering involving d.c. sputtering and d.c. bias sputtering; and Ramarotafika et al. is directed to forming WTi and WTi-N films by r.f. magnetron sputtering with d.c. substrate bias. There is no motivation to combine the various teachings of these references directed to different methods with different operating conditions.

In addition, claim 18 further recites that the program includes instructions for depositing a plurality of the first layers and second layers until the desired thickness of the film is reached. The references do not disclose or suggest depositing a plurality of first layers by sputtering without biasing the plasma and second layers by sputtering and biasing the plasma.

For at least the foregoing reasons, Applicants respectfully submit that claim 17 and claims 18 and 25-28 depending therefrom are patentable.

Claims 32-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al.

Applicants respectfully assert that independent claim 32 is patentable over the cited references because, for instance, they do not teach or suggest a second set of computer instructions for controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into said processing chamber to deposit a first layer of a film over a substrate by sputtering without biasing said plasma towards said substrate; and a third set of computer instructions for controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said processing chamber and to bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

The Examiner recognizes that Ye et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then

depositing a second layer over the first layer by sputtering and biasing the plasma. The remaining references do not cure the defects of Ye et al. and Onuki et al. Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight.

For at least the foregoing reasons, Applicants respectfully submit that claim 32 and claims 33-34 are patentable.

Claims 19-24, 29-31, 35, and 36

Claims 19, 29, 30, and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Claims 19 and 29 depend from claim 17 and further recite silicon and oxygen in the process gas. Claim 30 depends from claim 17 and further recites that the plasma generating system includes a first electrode, a second electrode, and a coil disposed about the vacuum chamber, and that the pedestal includes the second electrode. Claim 31 depends from claim 19 and recites that the silicon source contains silane. Applicants believe claims 19, 29, 30, and 31 are patentable for at least the same reasons that claim 17 is patentable. For instance, the references do not teach or suggest depositing a first layer by sputtering without biasing the plasma and a second layer by sputtering and biasing the plasma generated from a process gas having silicon and oxygen. Matsuura merely discloses formation of silicon oxide films, and does not cure the defects of the other references. Therefore, claims 19, 29, 30, and 31 are patentable.

Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. The references are directed to very different processes for forming different films to achieve different purposes. For example, Onuki et al. is directed to forming sputtered Al and Al alloy films using switching bias sputtering involving d.c. sputtering and d.c. bias sputtering; Ramarotafika et al. is directed to forming WTi and WTi-N films by r.f. magnetron sputtering with d.c. substrate bias; and Matsuura relates to deposition of silicon oxide films by plasma CVD. There is no suggestion that the operating conditions for depositing silicon oxide layers in Matsuura can be combined with the switching bias sputtering technique taught in Onuki et al.

Claims 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. The Examiner recognizes that Ye et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. The remaining references do not cure the defects of Ye et al. and Onuki et al. Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. Accordingly, claims 20-22 are patentable.

Claims 23, 24, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Applicants respectfully assert that claim 23 is patentable over the references because, for instance, the references do not teach or suggest an insulating layer formed between the metal layer and the semiconductor substrate and including a first silicon oxide layer and a second silicon oxide layer deposited using a high-density plasma chemical vapor deposition process, where the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer.

Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness, since the Examiner has not pointed to anything in the references that would suggest the claimed invention. Neither Onuki et al. nor Ramarotafika et al. teach depositing silicon oxide layers. Matsuura discloses silicon oxide layers, but fails to teach or suggest a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer.

Although Onuki et al. at Fig. 4 shows a SiO_2 layer, it is "thermally grown," not by high-density plasma chemical vapor deposition process. In addition, Onuki et al. does not teach or suggest two silicon oxide layers, wherein the first silicon oxide layer is deposited for the

reduction of mechanical stress in the second silicon oxide layer. The references do not, individually or combined, teach or suggest depositing first and second silicon oxide layers by high-density plasma chemical vapor deposition, where a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer.

For at least the foregoing reasons, Applicants respectfully assert that claim 23 and claims 24 and 36 depending therefrom are patentable.

In addition, claim 24 further recites that a second metal layer is formed above the substrate and below the at least one insulating layer, and a second insulating layer is formed between the second metal layer and the substrate. These features are also missing from the references.

Claim 36 further recites that the first silicon oxide layer is deposited on the substrate by applying a sputtering power to reactants to generate a plasma in a process chamber, and the second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants.

As discussed above, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. The remaining references do not cure the defects of Onuki et al. Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight.

Claim 35 depends from claim 32, and stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Claim 35 is patentable for at least the same reasons that claim 32 is patentable as discussed above. Matsuura merely discloses formation of silicon oxide films, and does not cure the defects of the other references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

Chun-Pok Leung
Reg. No. 41,405

TOWNSEND and TOWNSEND and CREW LLP
Tel: 650-326-2400
Fax: 415-576-0300
RL:asb:mmb
60090378 v1